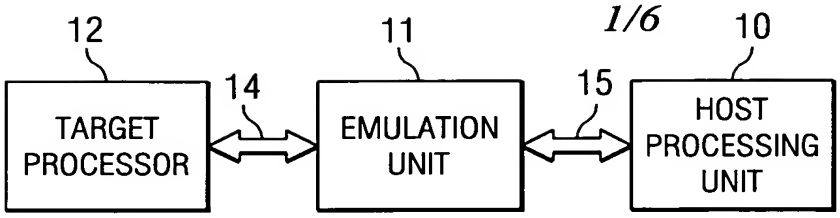

FIG. 1A

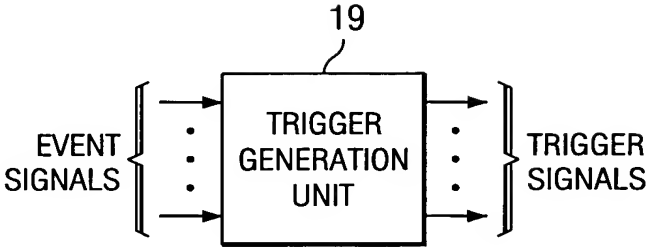

FIG. 1B

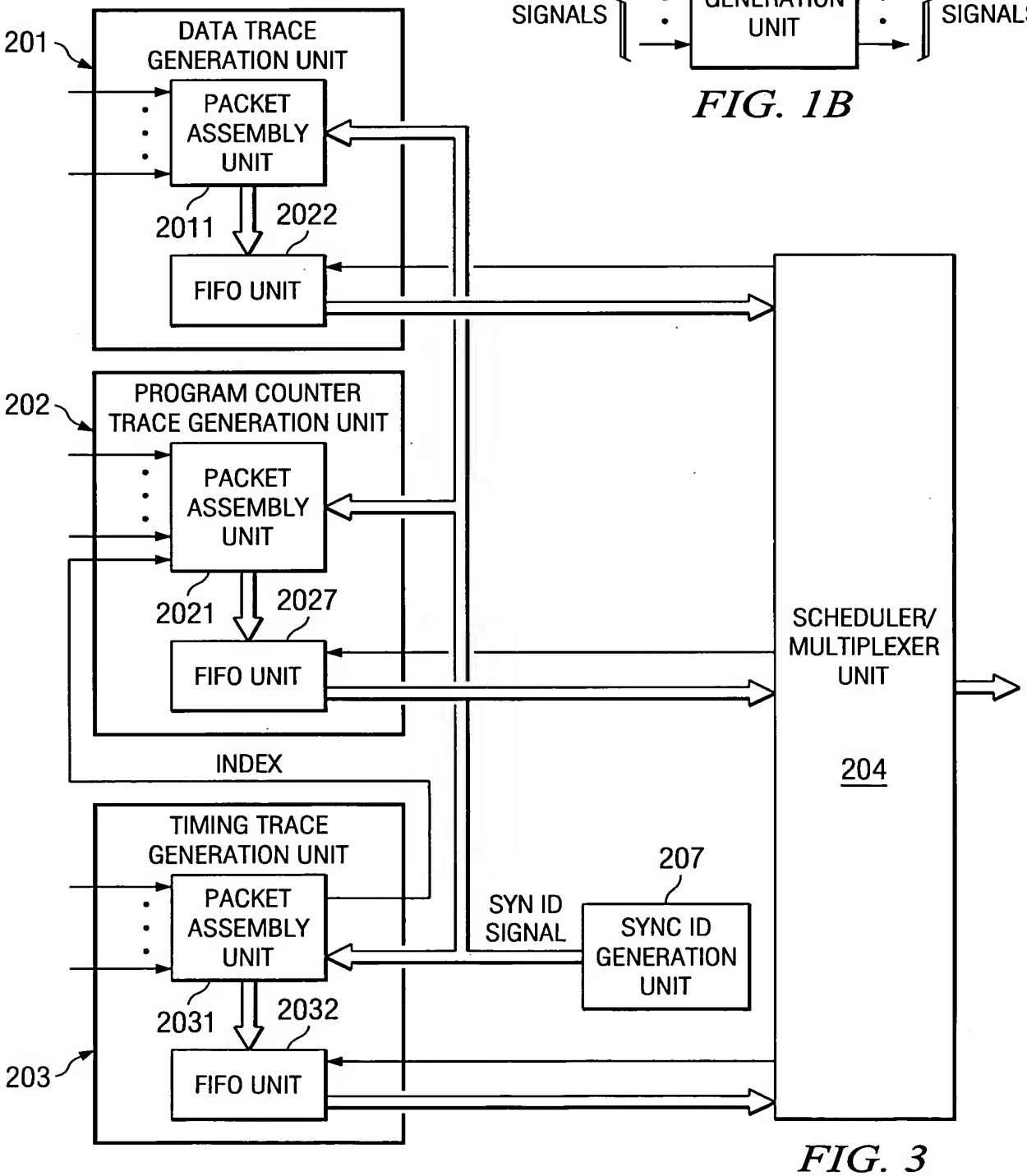

FIG. 3

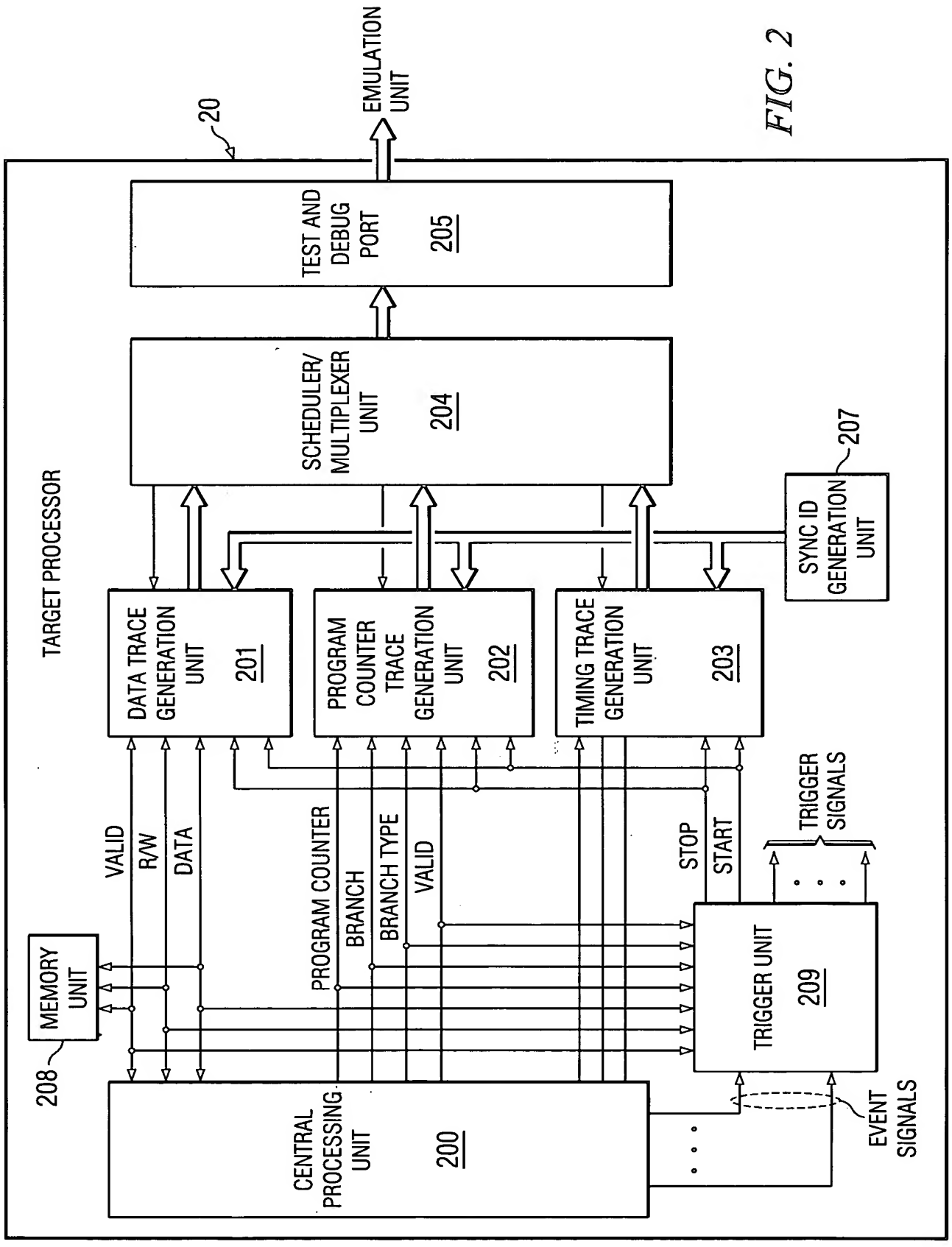
20
EMULATION UNIT
TEST AND DEBUG PORT 205
SCHEDULER/ MULTIPLEXER UNIT 204
TARGET PROCESSOR
207
SYNC ID GENERATION UNIT
DATA TRACE GENERATION UNIT 201
PROGRAM COUNTER TRACE GENERATION UNIT 202
TIMING TRACE GENERATION UNIT 203
VALID
R/W
DATA
PROGRAM COUNTER
BRANCH
BRANCH TYPE
VALID
STOP
START
TRIGGER SIGNALS
MEMORY UNIT
208
TRIGGER UNIT 209
CENTRAL PROCESSING UNIT 200
EVENT SIGNALS

FIG. 2

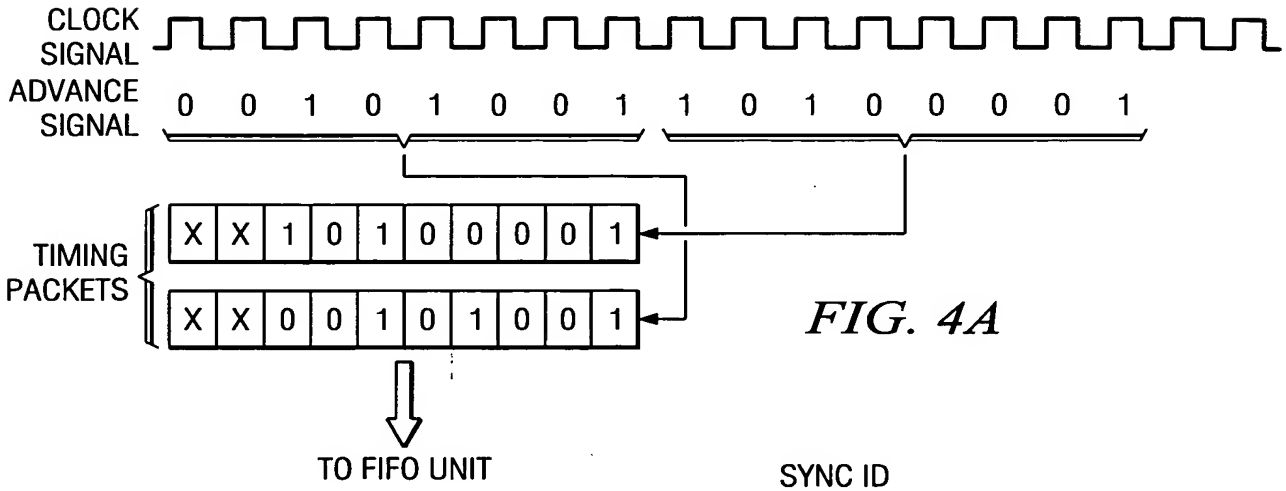

FIG. 4A

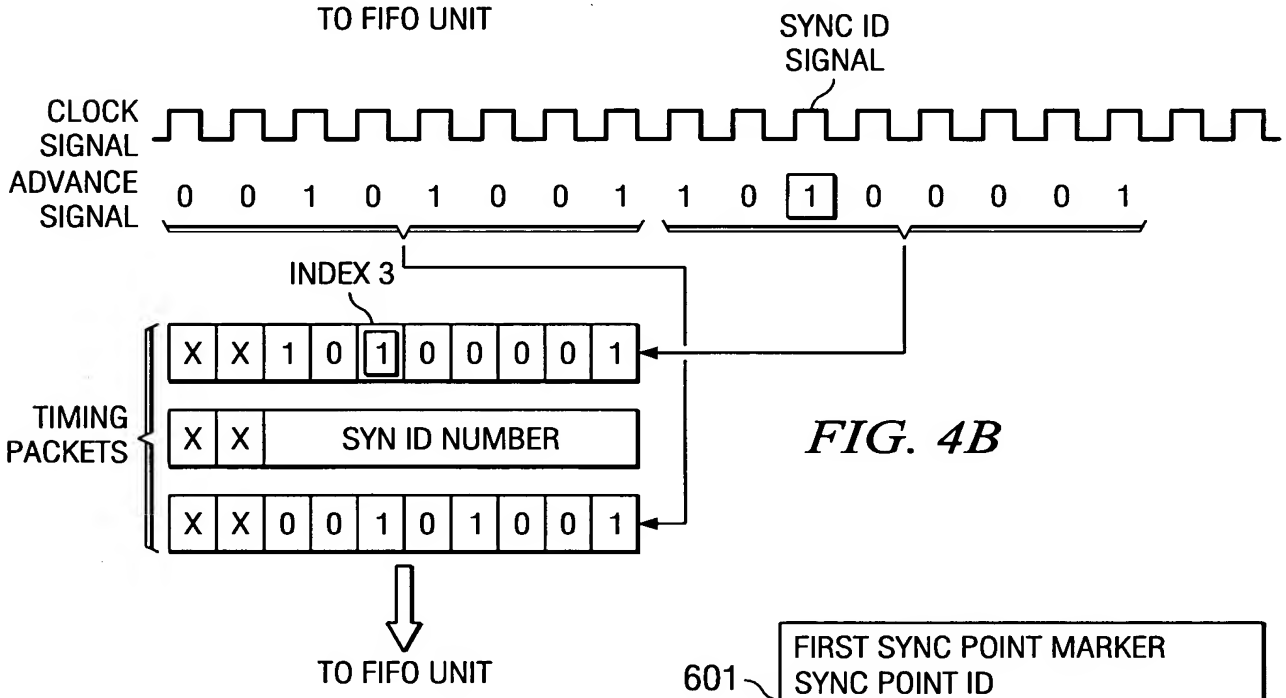

FIG. 4B

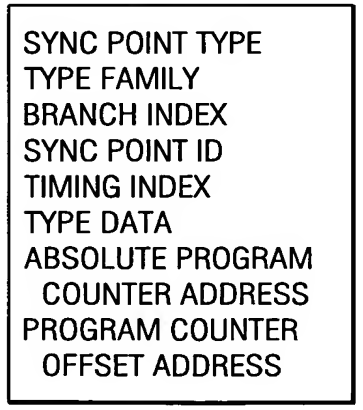

FIG. 5

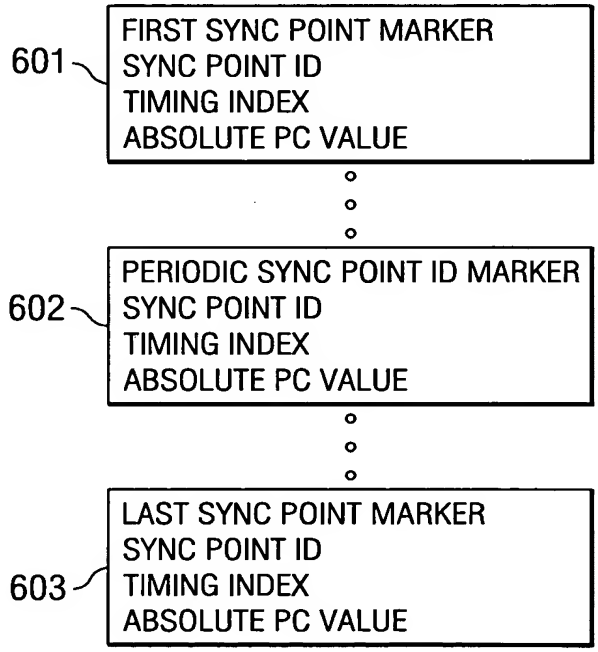

FIG. 6A

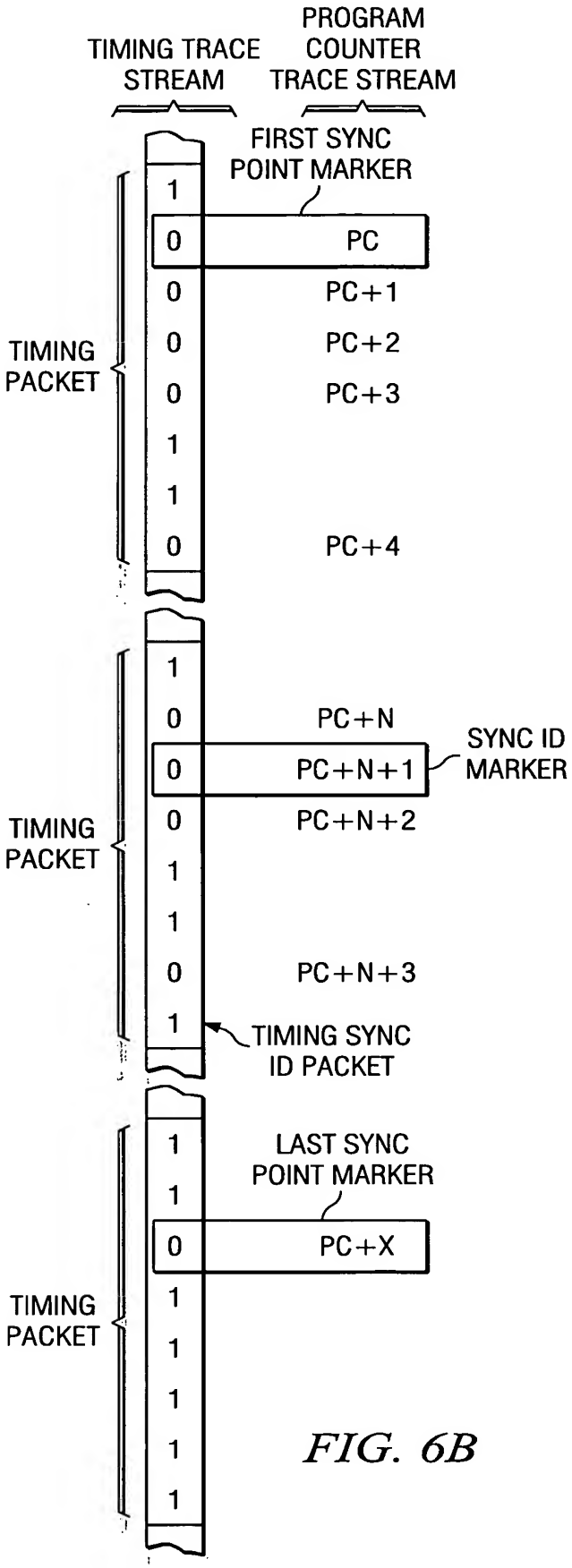
TIMING TRACE STREAM
PROGRAM COUNTER TRACE STREAM
FIRST SYNC POINT MARKER
1
0
PC
0
PC+1
0
PC+2
0
PC+3
1
1
0
PC+4
TIMING PACKET
1
0
PC+N
0
PC+N+1
SYNC ID MARKER
0
PC+N+2
1
1
0
PC+N+3
1
TIMING SYNC ID PACKET
TIMING PACKET
1
1
LAST SYNC POINT MARKER
0
PC+X
1
1
1
1
1

FIG. 6B

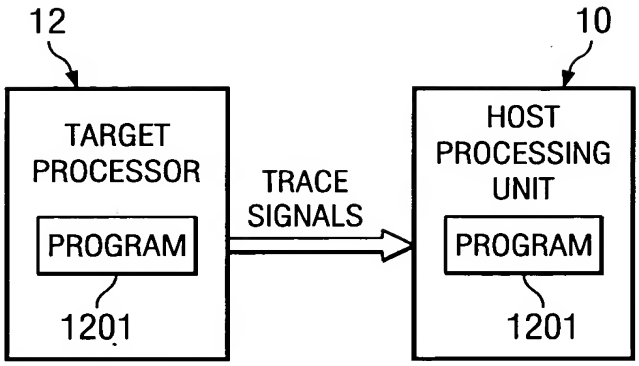
12
10
TARGET PROCESSOR
PROGRAM
1201
TRACE SIGNALS
HOST PROCESSING UNIT
PROGRAM
1201

FIG. 7

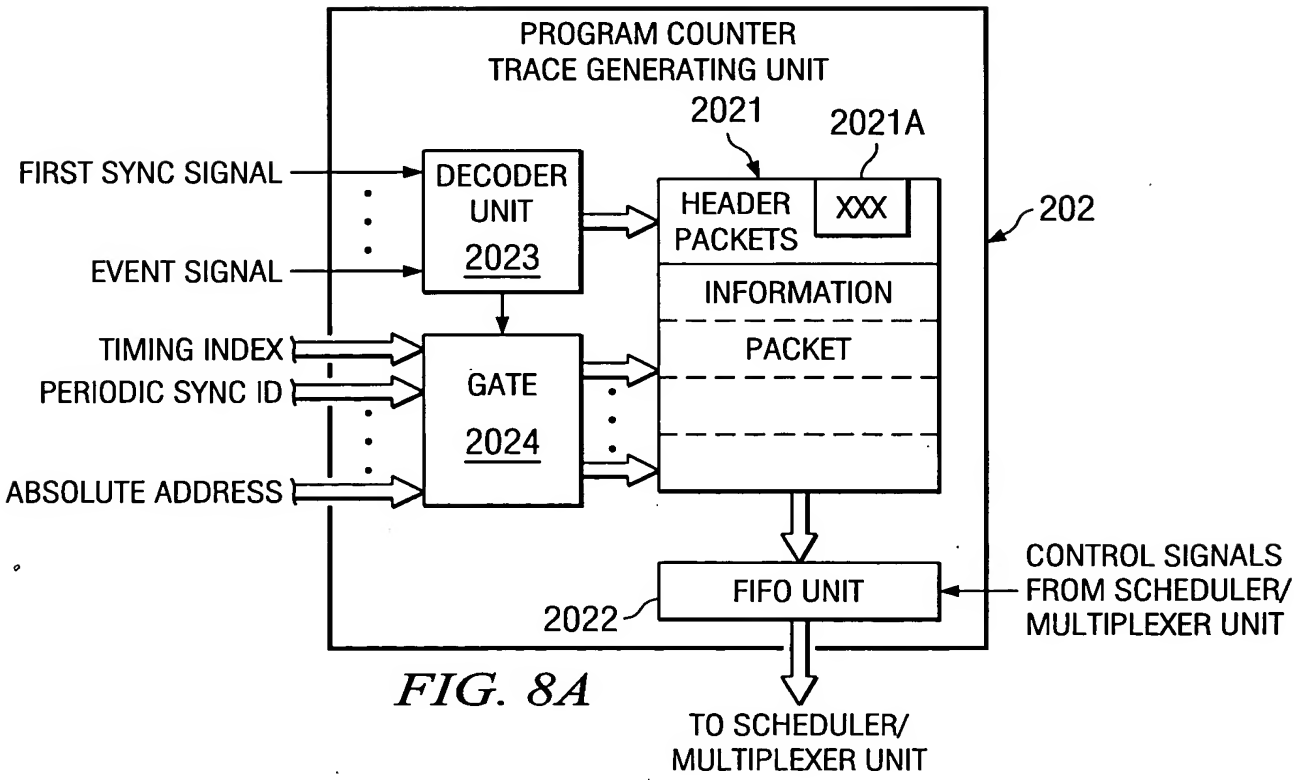
PROGRAM COUNTER TRACE GENERATING UNIT
2021
2021A
FIRST SYNC SIGNAL
EVENT SIGNAL
DECODER UNIT
2023
HEADER PACKETS
XXX
202
INFORMATION
PACKET
TIMING INDEX
PERIODIC SYNC ID
ABSOLUTE ADDRESS
GATE
2024
FIFO UNIT
2022
CONTROL SIGNALS FROM SCHEDULER/ MULTIPLEXER UNIT
TO SCHEDULER/ MULTIPLEXER UNIT

FIG. 8A

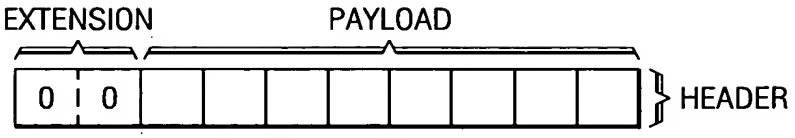

FIG. 9A

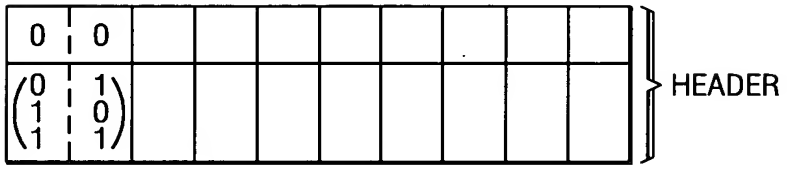

FIG. 9B

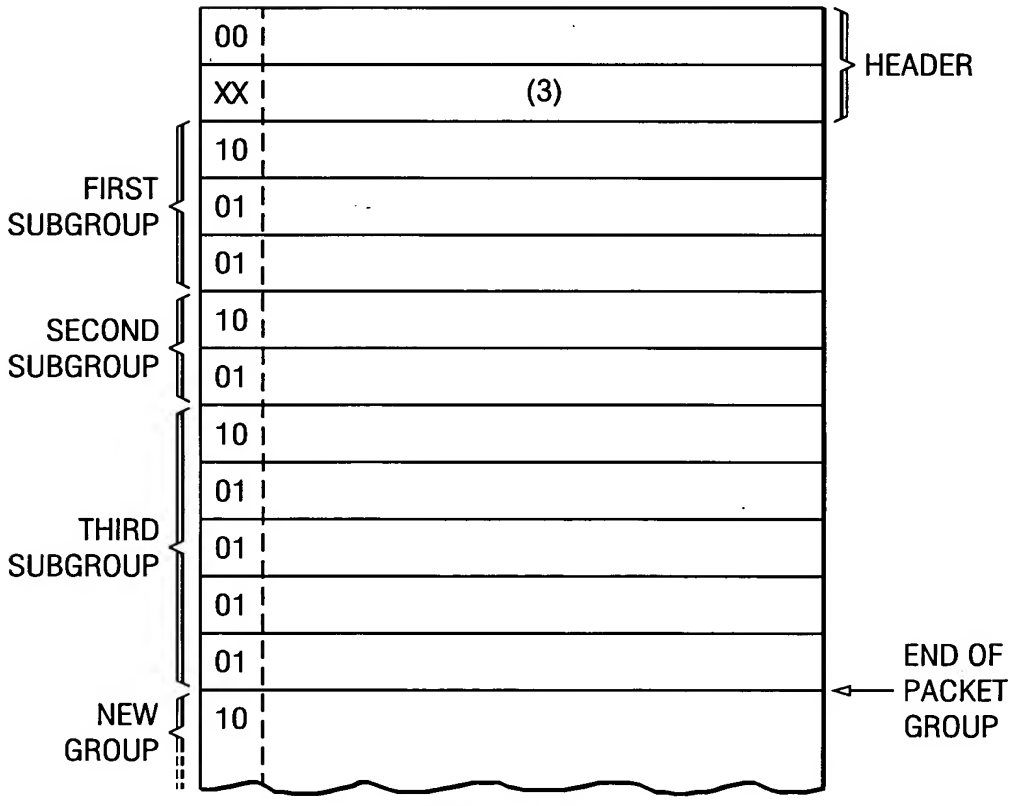

FIG. 9C